

DESIGN OF HIGH SPEED AND LOW POWER VOLTAGE LEVEL SHIFTER IN DUAL SUPPLY APPLICATIONS

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ABSTRACT

This paper presents an efficient and low-power voltage level shifter for enhanced performance in dual-supply applications. The proposed circuit's efficiency is based on the fact that the strength of the pull-up device is lowered while the pull-down device pulls the output down. At the same time, the pull-down device's strength is increased by an auxiliary circuit that consumes low power. The proposed circuit is simulated in 0.18 μ m technology Cadence Virtuoso software. The simulation results show that the proposed circuit can convert extremely low level of input voltage into high output voltage level. That is, it can convert low input voltage $V_{DDL}=0.8V$ to high output voltage $V_{DDH}=3V$ with power dissipation of 8.7 μ W.

Keywords—Voltage Level shifter, low power, Efficiency, power dissipation, voltage range.

I. INTRODUCTION

Static power dissipation and dynamic power dissipation are some sources of power consumption. In digital circuits, we can reduce this static power and dynamic power dissipation by reducing the power supply voltage. But the propagation delay of circuits increases while lowering the power supply voltage. In moderate-speed digital circuits or mixed-signal circuits, some parts operate at high speed; while some parts operate at low speed. In such circuits, instead of reducing the power supply voltage, we can use dual-supply architectures in which two supply voltages are used: low supply voltage (V_{DDL}) and high supply voltage (V_{DDH}). V_{DDL} is supplied for blocks that operate at low speed, i.e., that are in non-critical paths and (V_{DDH}) is applied for those digital blocks that operate at high speed, i.e., in critical paths. In such a digital system with dual-supply architectures, voltage level shifter circuits are necessary so that they can convert the lower voltage levels into higher voltage levels to provide the needed voltage levels for the next blocks. To enhance the performance of the dual-supply systems, and to avoid the degradation of their performance, the voltage level shifters used should be designed with reduced propagation delay, low power consumption and reduced silicon area. And also to save more power, the voltage level shifters

should be capable of converting very low V_{DDL} values to values below the input transistors' threshold voltage. Therefore, in this paper, an efficient and low power voltage level shifter is proposed. This proposed shifter can convert even very low input voltages into high voltages at the output. The remaining of this paper is structured as follows. Analysis of some conventional voltage level shifters is given in Section II. Introduction of the proposed level shifter in Section III. Simulation results of the proposed circuit are presented in Section IV. Lastly, conclusion in Section V.

II. EXISTING SYSTEM

Some of the conventional voltage level shifters are shown in Fig.1. Fig.1a shows a conventional voltage shifter. Its operation is given below. When the input IN is high, i.e., $IN=V_{DDL}$, the transistor MN1 is ON and pulls down the node Q1; MN2 is OFF. Next, MP2 is slowly turned ON and pulls up the node Q2 to V_{DDH} and then turns OFF MP1. Similarly, When the input IN is low, i.e., $IN=V_{SS}$, the operation is reversed. It is observed that in this circuit, contention is present at the nodes Q1 and Q2 between the PMOS devices (MP1 and MP2) which are supplied by V_{DDH} and the NMOS devices (MN1 and MN2) supplied by V_{DDL} . So, when the difference between V_{DDL} and V_{DDH} is high, and when the input voltage is below the threshold range, this conventional circuit cannot convert the

the output node up and MP3 turns OFF. Also, MN4 gate is pulled down which means that there is no static current through MP1, MN1 and MN4. If the aspect ratio of MP1 is chosen smaller than the aspect ratio of MP2, the power consumption can be reduced. During the transition of input signal from high to low, MN2 turns ON and MN1 turns OFF at the same time. Hence, there is no transition current through MP1. Thus, the strength of pull-up device MP2 when the pull-down device pulls the output down. Therefore, the delay, contention and power consumption are reduced. Also, the shifter can correctly work for input voltages in the subthreshold range. This principle is made possible using an auxiliary circuit in the proposed circuit. The auxiliary circuit consists of six transistors MN5, MN6, MN7 and it turns ON only when the input signal changes from high level to low level.

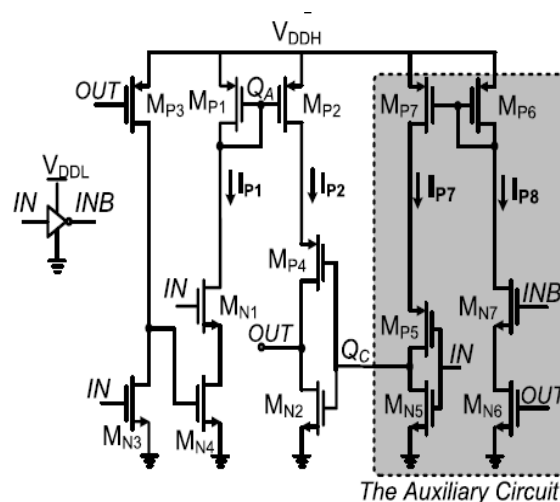


Fig.2. Proposed voltage level shifter.

The auxiliary circuit's operation is as follows. When the input goes low, and when the output does not correspond to input, MN5 turns OFF and MP6, MN6, MN7 are ON. Thus, a transition current will flow through MP6, MN6 and MN7. This current is mirrored into MP7 which pulls the node QC . That is MN2 turns ON and MP4 turns OFF and the contention is reduced significantly. When the output is pulled down to ground, MN6 turns OFF and no current is flowing through MP6, MN6 and MN7 which means that the auxiliary circuit is ON only for the transition of the input from high level to low level. Thus the contention is negligible and the propagation delay and power consumption are reduced significantly.

IV. EXPERIMENTAL RESULTS

The proposed level shifter (Fig.2) and conventional level shifters (Fig.1(a) and (b)) have been simulated in Cadence Virtuoso platform in 0.18- μm CMOS technology.

The simulation and experimental results are shown below.

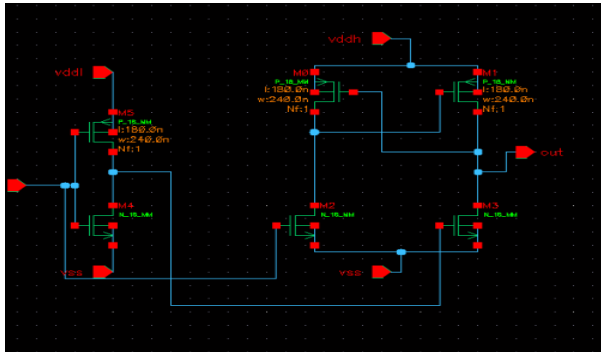


Fig.3. Implementation of schematic of conventional level shifter (Fig.1(a))

In the above-shown level shifter, V_{DDL} of 1.5V and V_{DDH} of 3V are applied and the circuit is simulated in Cadence tool. The simulation result is shown below in Fig.4.

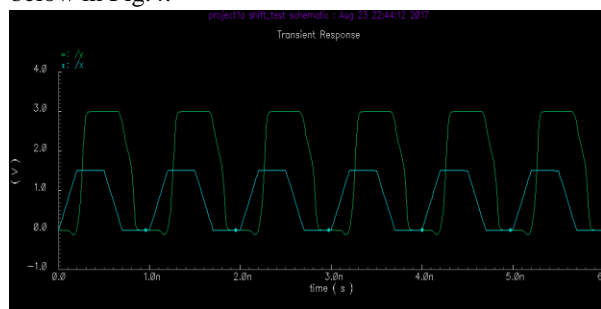


Fig.4. Simulation result of Fig.1(a).

The level shifter with semi-static current mirror shown in Fig.1 (b) is implemented in Cadence tool and shown below.

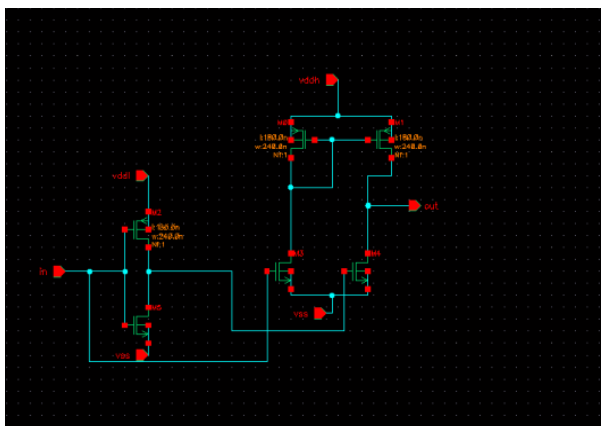


Fig.5. Implementation of schematic of level shifter with current mirror (Fig.1(b)).

For the above circuit, V_{DDL} of 1V and V_{DDH} of 3V are applied and simulated. The simulation result is shown below which shows that it can convert input voltage of 1V to 3V at the output.

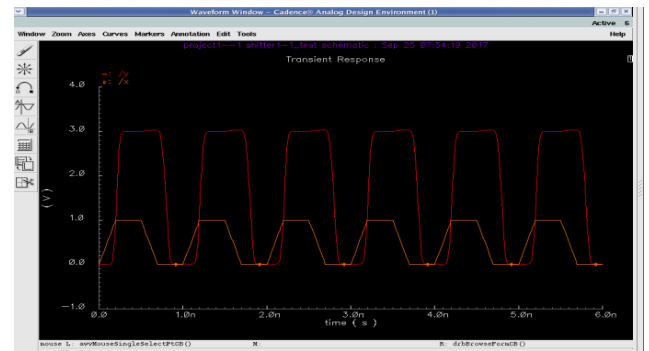


Fig.6. Simulation result of Fig.1(b).

The power consumption of voltage level shifter given in Fig.1(b) is reduced and is lower than that of Fig.1(a). The conventional voltage level shifter (Fig.1(a)) can convert input voltages from 1.5V; it cannot convert input voltage below 1.5V. This is overcome by the level shifter in Fig.1(b) which can convert input voltage of lower than 1.5V.

The proposed level shifter shown in Fig.2 can be able to convert extremely low input voltages also and its simulation is shown below.

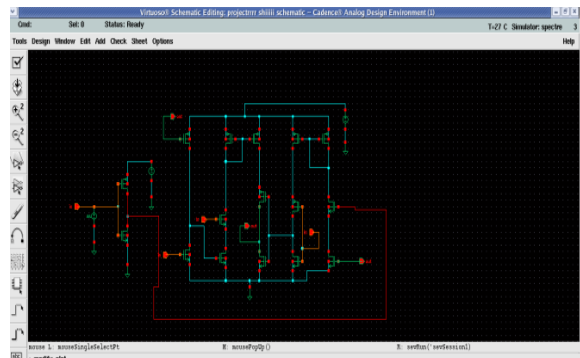


Fig.7. Implementation of schematic of proposed level shifter (Fig.2).

In the proposed level shifter, V_{DDL} value is 0.8V and V_{DDH} value is 3V. The simulation of above circuit shows that the circuit is capable of converting even low input voltage of 0.8V to high output voltage of 3V which is shown below.

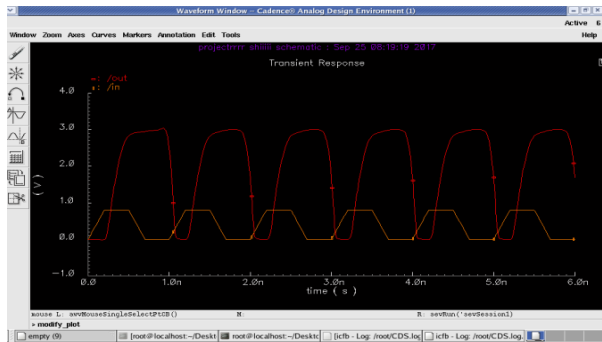


Fig.8. Simulation result of proposed level shifter.

The following table shows the comparison of power consumption of the conventional level shifters and the proposed voltage level shifter.

Table 1. Comparison of simulation results of the conventional and proposed level shifters.

Type	VDDL	VDDH	V _{in}	V _{out}	Power for VDDL=1.5 V
Fig.1(a)	1.5V	3V	1.5 V	3V	453.543μW
Fig.1(b)	1V	3V	1V	3V	63.0609μW
Fig2	0.8V	3V	3V	3V	8.7198 μW

Table I summarizes the power consumption of the structures shown in Fig.1(a), 1(b) and Fig.2. The power consumption of the proposed level shifter is reduced and is lower than the conventional level shifters. Also, the proposed level shifter can convert even extremely low level of input voltages compared to the conventional ones.

V. CONCLUSION

In this paper, an efficient and low-power voltage level-shifter design was proposed. This proposed shifter can convert extremely low level of input voltages. The power consumption of the proposed circuit is also reduced significantly. The simulation and experimental results show that the proposed level shifter is efficient compared to the other existing level shifters.

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